CLAIMS

WHAT IS CLAIMED IS:

1. A bus interface logic configured with a storage location configured to store a master mode bit, wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set.

2. The bus interface logic of claim 1 further configured to flush output buffers in response to the master mode bit being reset.

3. The bus interface logic of claim 1 further configured to operate normally after the master mode bit is reset.

4. The bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses, and wherein the bus interface logic is configured to exchange data only with the one or more addresses.

5. The bus interface logic of claim 4, wherein the one or more addresses comprise an address range, wherein the bus interface logic is configured to exchange data only within the address range.

6. The bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses, and wherein the bus interface logic is configured not to exchange data with the one or more addresses.

7. A computer system, comprising:

a master device configured to set and reset a master mode bit; and

one or more bus interface logics, each configured with a storage location configured to store the master mode bit, wherein the bus interface logics are configured to exchange data only with the master device when the master mode bit is set.

8. The computer system of claim 7, wherein the bus interface logics are further configured to flush output buffers in response to the master mode bit being reset.

9. The computer system of claim 7, wherein the one or more bus interface logics are further configured to operate normally after the master mode bit is reset.

10. The computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logics are configured to exchange data only with the one or more addresses.

11. The computer system of claim 10, wherein the one or more addresses comprise an address range, wherein the one or more bus interface logics are configured to exchange data only within the address range.

12. The computer system of claim 10, wherein the master device is further configured to store the one or more addresses in the storage location along with the master mode bit.

13. The computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logic are configured not to exchange data with the one or more addresses.

14. The computer system of claim 10, wherein the master device is further configured to store the one or more addresses in the storage location along with the master mode bit.

15. The computer system of claim 7, further comprising:

a processor configured to exchange data through the one or more bus interface logics when the master mode bit is not set; and

wherein the one or more bus interface logics are further configured not to exchange data for the processor when the master mode bit is set.

16. The computer system of claim 7, wherein the master device comprises a crypto-processor.

17. The computer system of claim 7, wherein the master device comprises security hardware.

18. A computer system, comprising:

a master device;

a device, different from the master device, configured to provide authentication data to the master device;

at least a first bus interface logic coupled to the master device, wherein the first bus interface logic comprises a first storage location for storing a first master mode bit; and

at least a second bus interface logic coupled to the device, wherein the first bus interface logic comprises a second storage location for storing a second master mode bit;

wherein the master device is configured to cause to be set the first master mode bit in the first storage location and the second master mode bit in the second storage location;

wherein the first bus interface logic is configured to exchange data only between the master device and the second bus interface logic when the first master mode bit is set; and

wherein the second bus interface logic is configured to exchange data only between the device and the first bus interface logic when the second master mode bit is set.

19. The computer system of claim 18, wherein the master device is configured to set and reset the first and second master mode bits.

20. The computer system of claim 18, wherein the first and second bus interface logics are further configured to flush output buffers in response, respectively, to the first and second master mode bits being reset.

21. The computer system of claim 18, wherein the first and second bus interface logics are further configured, respectively, to operate normally after the first and second master mode bits are reset.

22. The computer system of claim 18, wherein the first and second storage locations are further each configured to store one or more addresses, and wherein the first and second bus interface logics are configured, respectively, to exchange data only with the one or more addresses as stored therein.

23. The computer system of claim 22, wherein the one or more addresses comprise an address range, wherein the first and second bus interface logics are configured to exchange data only within the address range.

24. The computer system of claim 22, wherein the master device is further configured to store the one or more addresses in the first and second storage locations along with the first and second master mode bits.

25. The computer system of claim 18, wherein the first and second storage locations are further configured to store one or more addresses, and wherein the first and second bus interface logics are each configured not to exchange data with the one or more addresses stored therein.

26. The computer system of claim 22, wherein the master device is further configured to store the one or more addresses in the first and second storage locations along with the first and second master mode bits.

27. The computer system of claim 18, further comprising:

a processor configured to exchange data through the first and second bus interface logics when the first and second master mode bits are not set; and

wherein the first and second bus interface logics are each further configured not to exchange data for the processor when the first and second master mode bits, respectively, are set.

28. The computer system of claim 18, wherein the master device comprises a crypto-processor.

29. The computer system of claim 18, wherein the master device comprises security hardware.

30. A method of operating a computer system, the method comprising:

setting a master mode bit for a bus interface logic;

passing a data request through the bus interface logic only for a specified device;

receiving data in response to the data request from the specified device; and

resetting the master mode bit.

31. The method of claim 30, further comprising:

setting a master mode bit in another bus interface logic; and

passing the data request from the another bus interface logic to the bus interface logic only for the specified device.

32. The method of claim 30, wherein setting a master mode bit for a bus interface logic comprises a master device setting the master mode bit for the bus interface logic; and

wherein passing the data request through the bus interface logic only for the specified device further comprises the master device providing the data request through the bus interface logic only for the specified device.

33. The method of claim 30, further comprising:

making an attempt to access the bus interface logic; and

rejecting the attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set.

34. The method of claim 30, further comprising:

resetting the master mode bit; and

flushing buffers of the bus interface logic in response to resetting the master mode bit.

35. The method of claim 34, further comprising:

making an attempt to access the bus interface logic; and

accessing the bus interface logic in response to making the attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset.

36. The method of claim 30, further comprising:

storing one or more address locations along with the master mode bit for the bus interface logic.

37. The method of claim 36, further comprising:

restricting data transmissions only to the one or more address locations.

38. The method of claim 36, further comprising:

restricting data transmissions only to within an address range defined by the one or more address locations.

39. The method of claim 36, further comprising:

restricting data transmissions from the one or more address locations.

40. The method of claim 36, further comprising:

restricting data transmissions from within an address range defined by the one or more address locations.

41. A computer system, comprising:

means for storing an indicator of a master mode;

means for restricting data transfers when the indicator of the master mode is set;

means for resetting the indicator of the master mode.

42. A computer system, comprising:

means for setting a master mode bit for a bus interface logic;

means for passing a data request through the bus interface logic only for a specified device;

means for receiving data in response to the data request from the specified device; and

means for resetting the master mode bit.

43. The computer system of claim 42, further comprising:

means for setting a master mode bit in another bus interface logic; and

means for passing the data request from the another bus interface logic to the bus interface logic only for the specified device.

44. The computer system of claim 42, further comprising:

means for rejecting an attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set.

45. The computer system of claim 42, further comprising:

means for resetting the master mode bit; and

means for flushing buffers of the bus interface logic in response to resetting the master mode bit.

46. The computer system of claim 45, further comprising:

means for accessing the bus interface logic in response to making an attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset.

47. A computer readable program storage device encoded with instructions that, when executed by a computer, performs a method of operating a computer system, the method comprising:

setting a master mode bit for a bus interface logic;

passing a data request through the bus interface logic only for a specified device;

receiving data in response to the data request from the specified device; and

resetting the master mode bit.

48. The computer readable program storage device of claim 47, the method further comprising:

setting a master mode bit in another bus interface logic; and

passing the data request from the another bus interface logic to the bus interface logic only for the specified device.

49. The computer readable program storage device of claim 47, wherein setting a master mode bit for a bus interface logic comprises a master device setting the master mode bit for the bus interface logic; and wherein passing the data request through the bus interface logic only for the specified device further comprises the master device providing the data request through the bus interface logic only for the specified device.

50. The computer readable program storage device of claim 47, the method further comprising:

making an attempt to access the bus interface logic; and

rejecting the attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set.

51. The computer readable program storage device of claim 47, the method further comprising:

resetting the master mode bit; and

flushing buffers of the bus interface logic in response to resetting the master mode bit.

52. The computer readable program storage device of claim 51, the method further comprising:

making an attempt to access the bus interface logic; and

accessing the bus interface logic in response to making the attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset.

53. The computer readable program storage device of claim 47, the method further comprising:

storing one or more address locations along with the master mode bit for the bus interface logic.

54. The computer readable program storage device of claim 53, the method further comprising:

restricting data transmissions only to the one or more address locations.

55. The computer readable program storage device of claim 53, the method further comprising:

restricting data transmissions only to within an address range defined by the one or more address locations.

56. The computer readable program storage device of claim 53, the method further comprising:

restricting data transmissions from the one or more address locations.

57. The computer readable program storage device of claim 53, the method further comprising:

restricting data transmissions from within an address range defined by the one or more address locations.